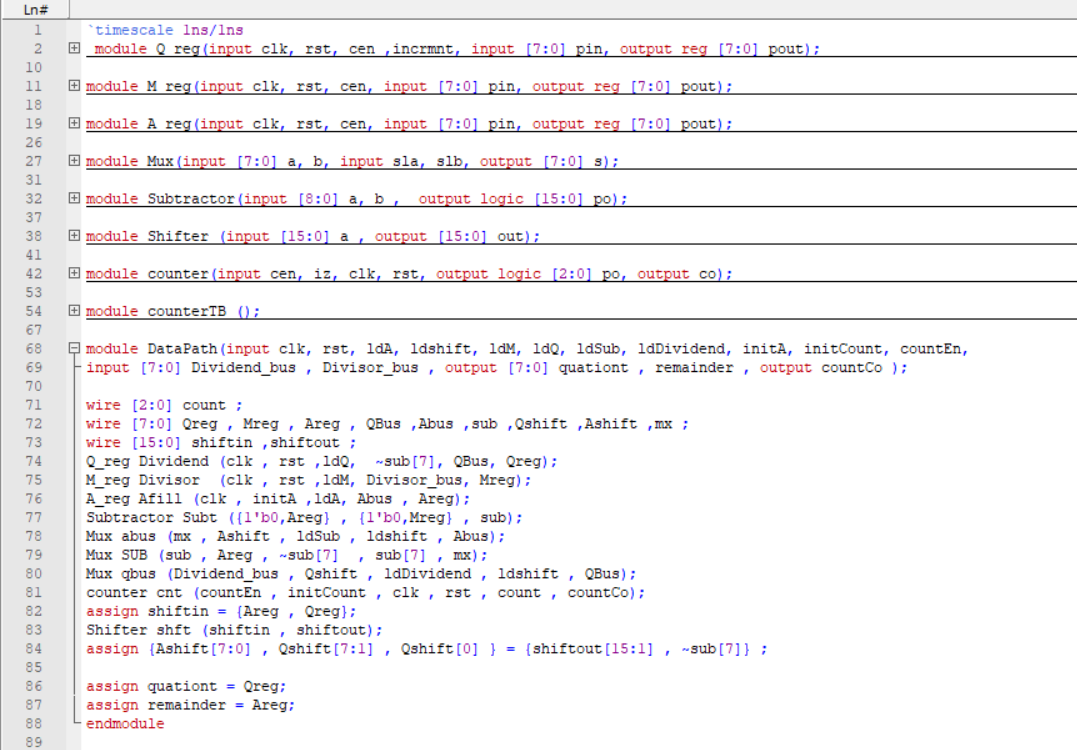
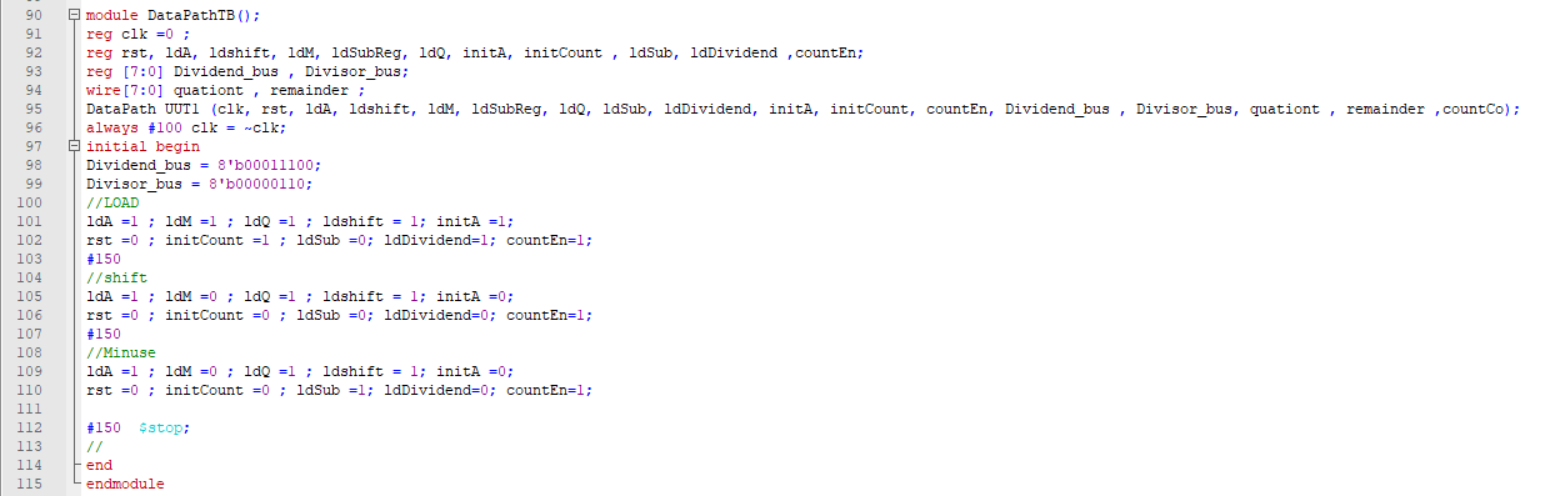
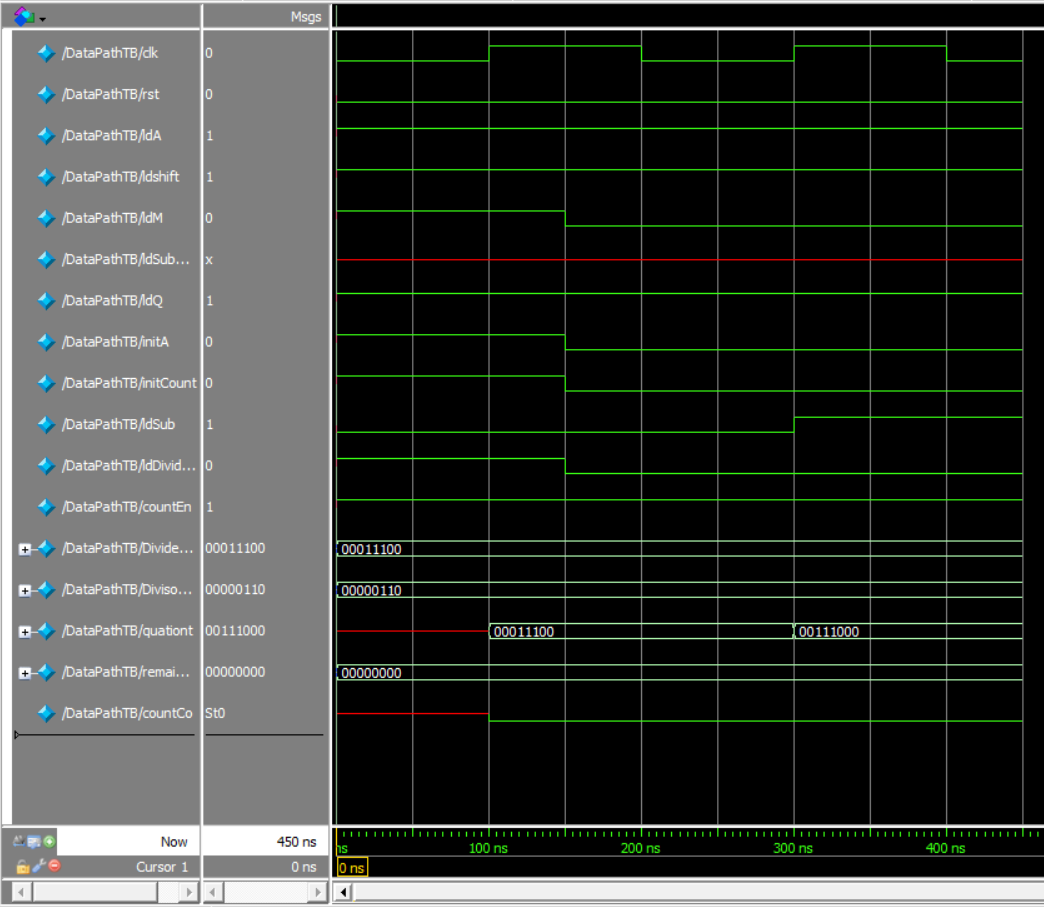
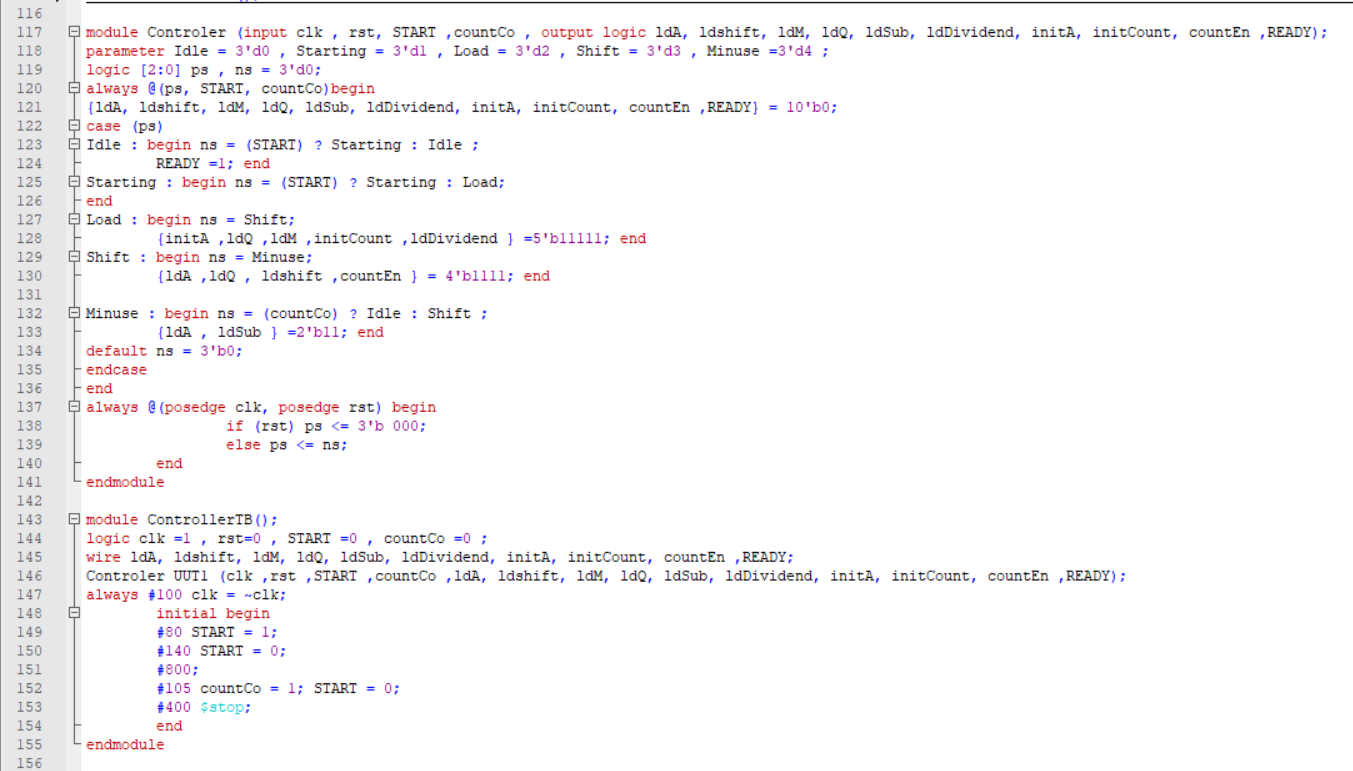
Amir Abbas Moumeni Zadeh – 810101529 – CA#5 – Digital Systems I ECE894

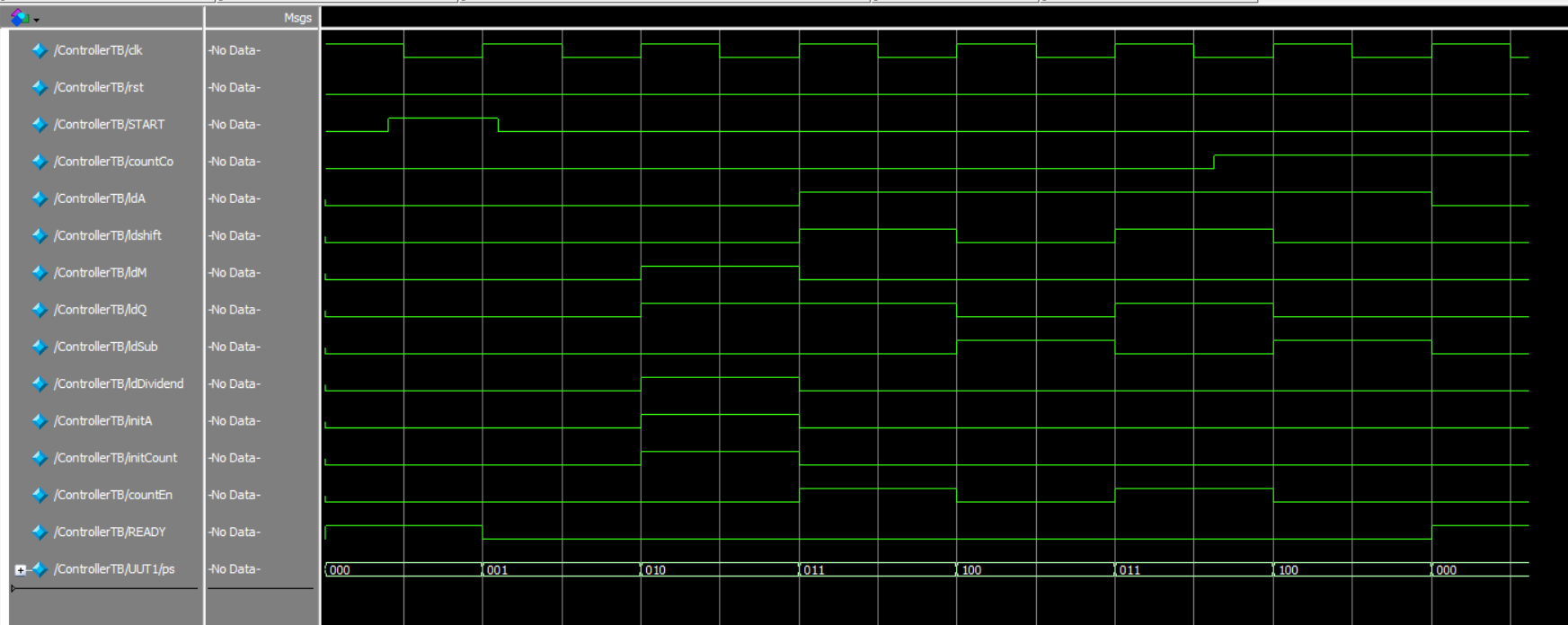
In this project we are going to design a **Divider** circuit.

DataPath Codes. Assuming all modules and wiring them together in DataPath module.

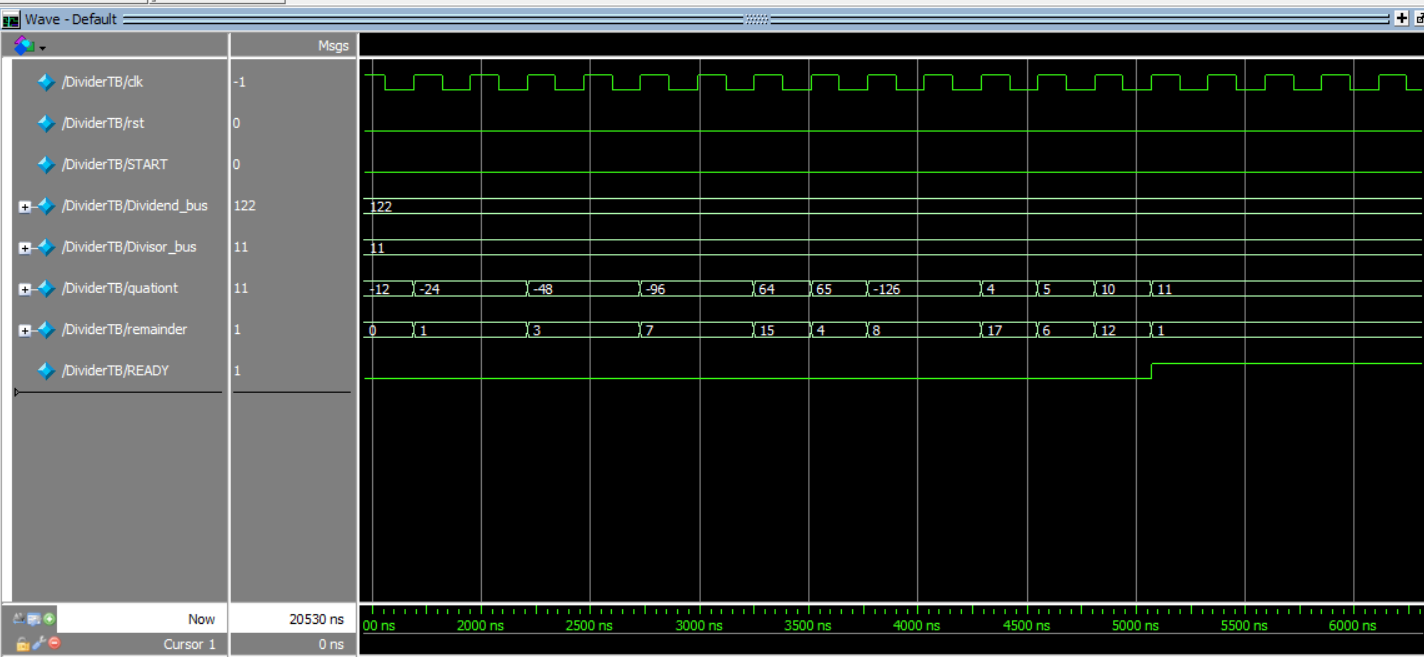
TestBench for DataPath. Assuming All control Signals that should come from controller manualy just to test the Functionality of circuit.

we have not connected the Controller Unit so we don’t expect Dividing from this circuit.

Hopefully DataPath is working Correcty.

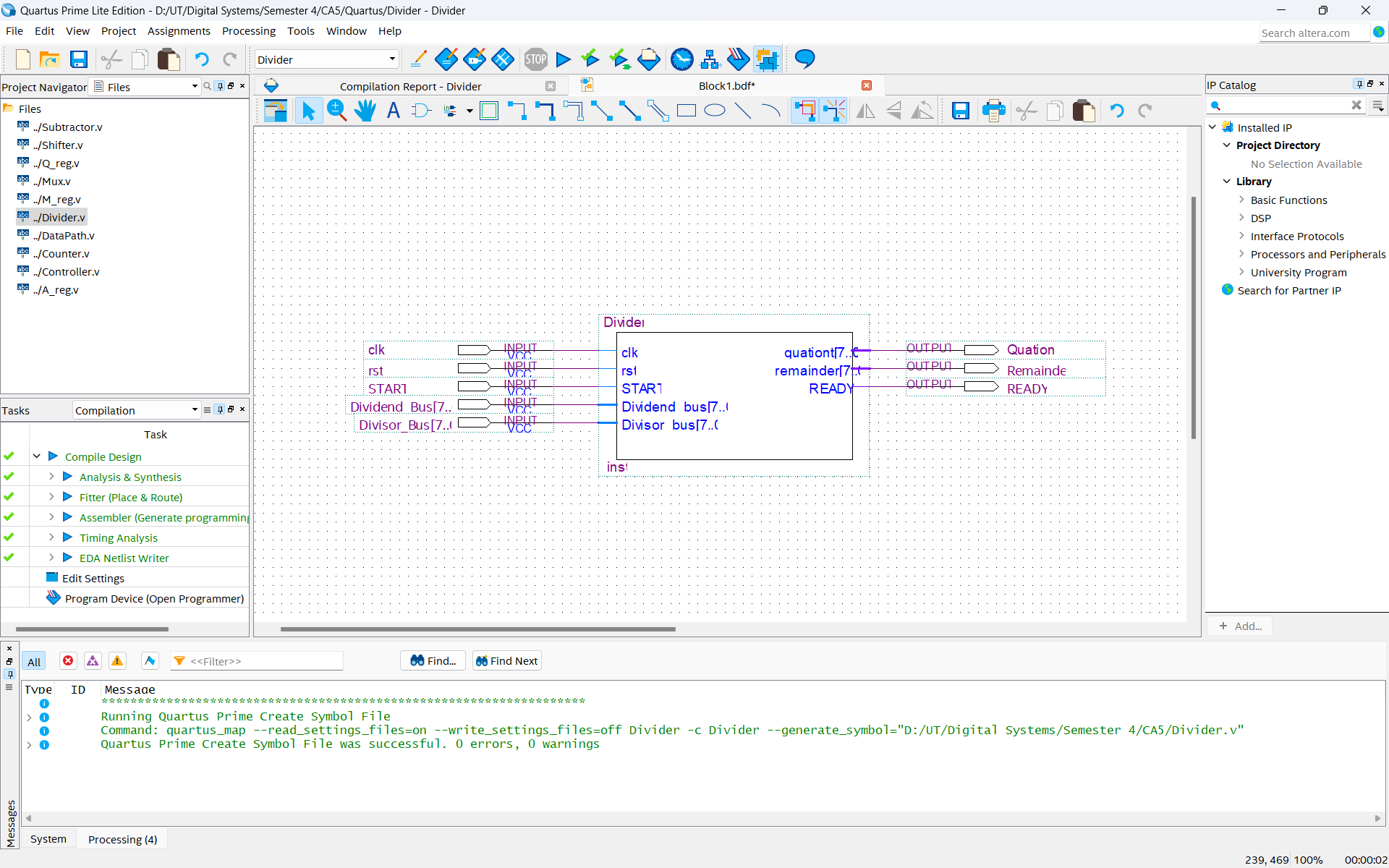
Assuming All Signals that should come from DataPath as inputs manualy just to test the Functionality of circuit.

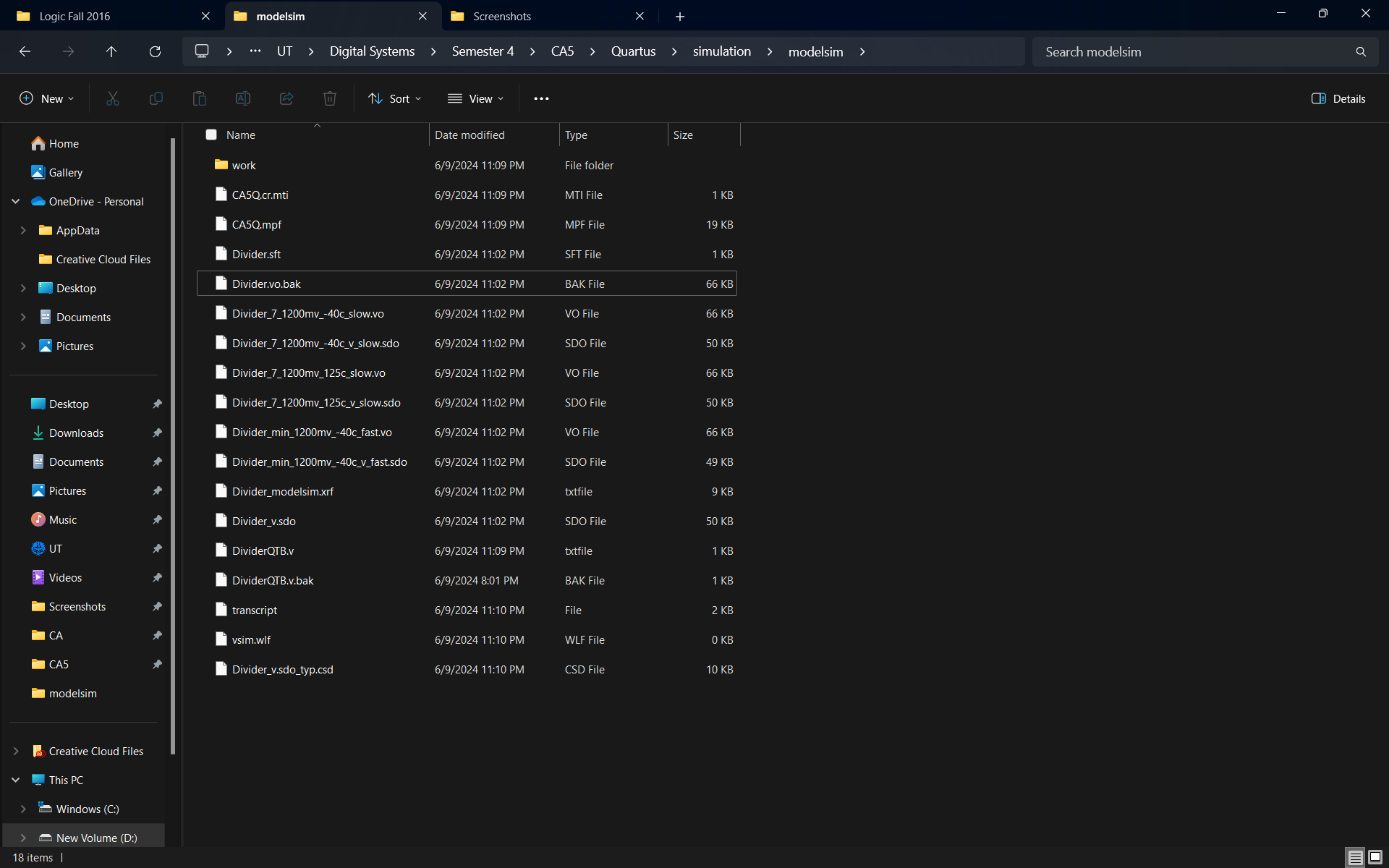
Aparantly Controller is Working Correctly. In each state control signals that we want are assuming.

Now connecting controler to DataPath should work correctly. Hopefully!

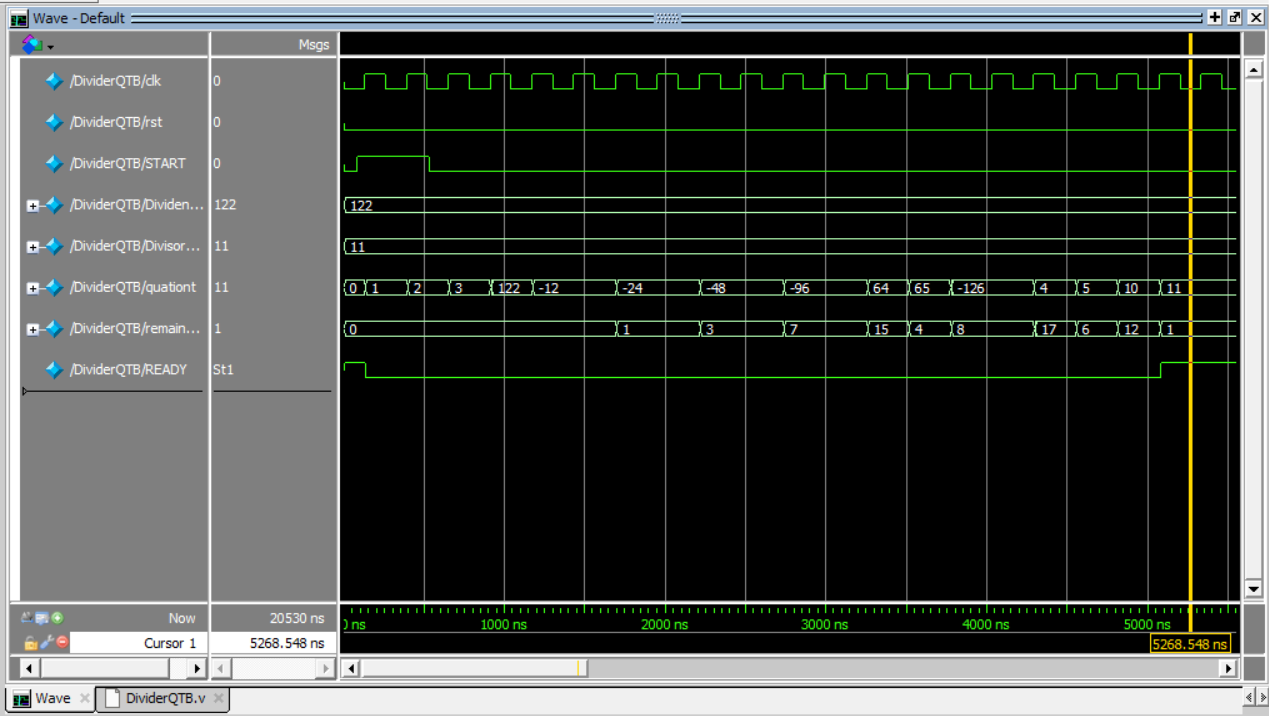
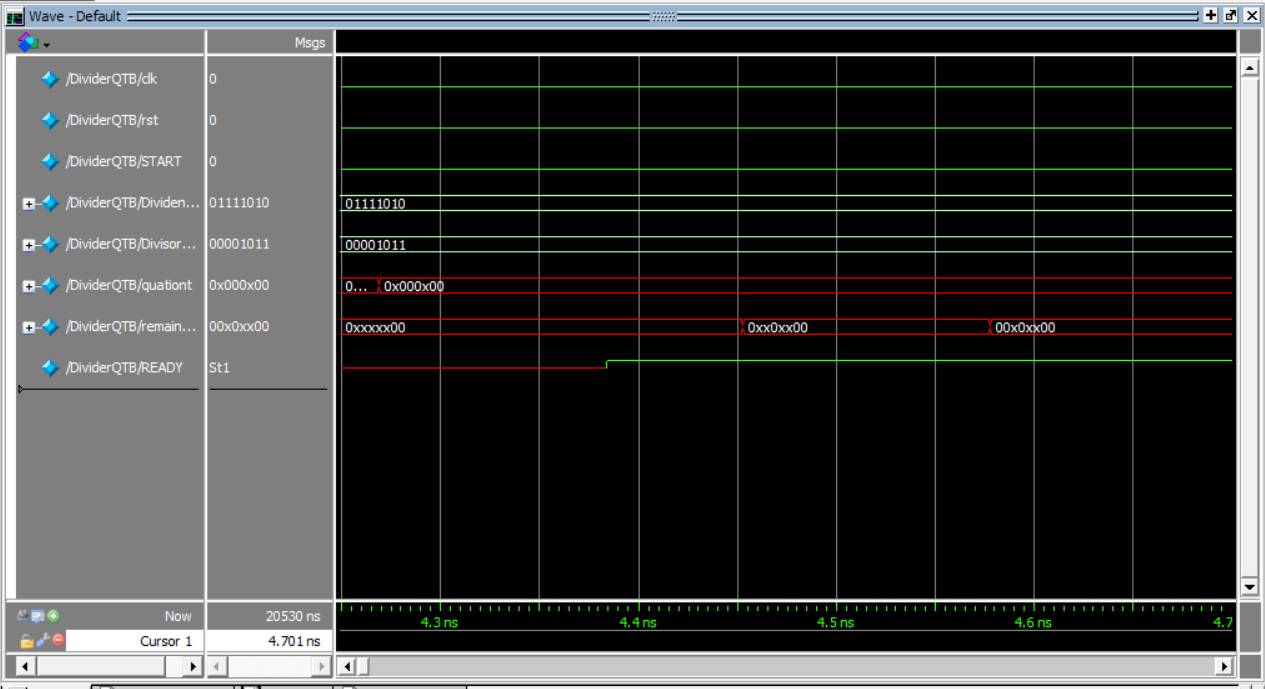
When the READY signal is turned on, we read the outputs and they are right according to inputs.

Beautifully Done!

**Quartus**

Symbol for Top level block diagram in quartus.

.sdo and .vo files are created.

in this simulation we can see timing is included.

Timing is obvious in this Waveform.

